Refine Search

Search Results -

Terms	Documents
L3 same ((external or remote) near5 (module or device or drive))	17

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, January 13, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L5	l3 same ((external or remote) near5 (module or device or drive))	17	L5
L4	L1 near10 control$4	1164	L4
L3	L1 near10 control$4	1164	L3
~~L2~~	~~L1 near10 control44~~	~~0~~	~~L2~~
L1	fabric near5 (connect$3 or switch$3)	9139	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L5	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, January 13, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5	0	L6
DB=USPT; PLUR=YES; OP=OR			
L5	l3 same ((external or remote) near5 (module or device or drive))	17	L5
L4	L1 near10 control$4	1164	L4
L3	L1 near10 control$4	1164	L3
~~L2~~	~~L1 near10 control$4~~	~~0~~	~~L2~~
L1	fabric near5 (connect$3 or switch$3)	9139	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 same external	13

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, January 13, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L3	L2 same external	13	L3
L2	L1 near10 control$4	413	L2
L1	(fabric near5 connect$3)	7295	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L2 same external	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

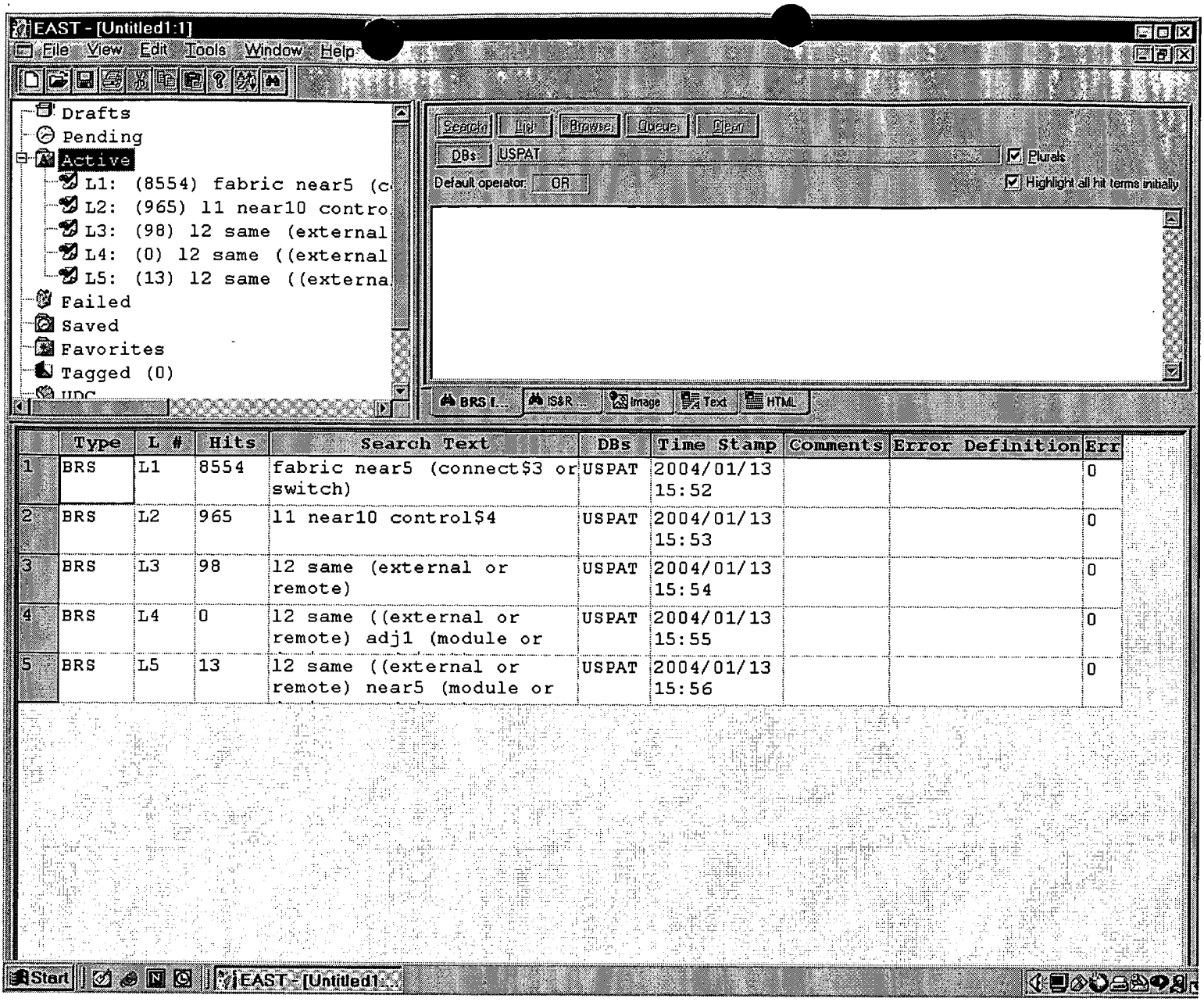
Recall Text | Clear | Interrupt

Search History

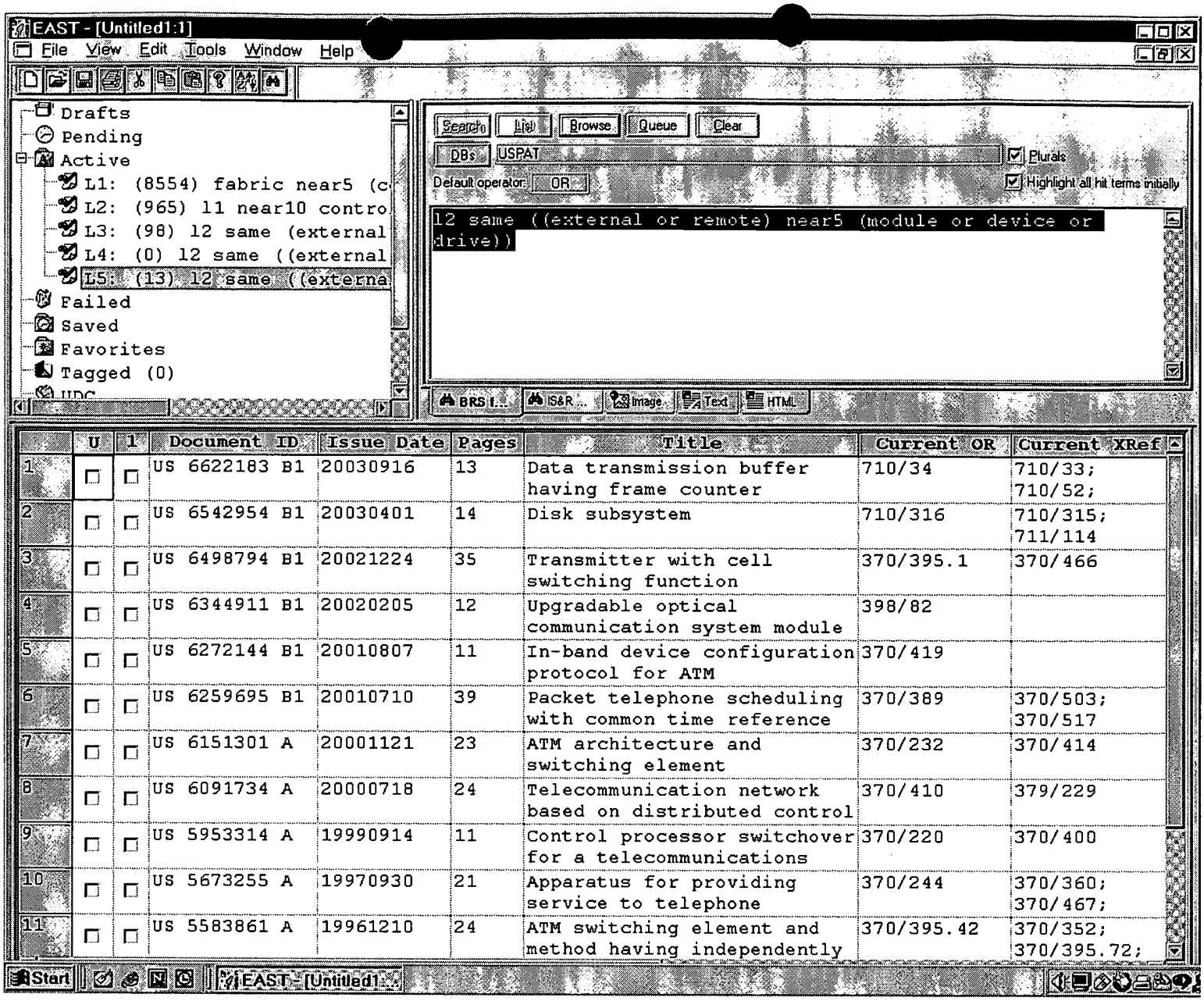
DATE: Tuesday, January 13, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L2 same external	0	L4
DB=USPT; PLUR=YES; OP=OR			
L3	L2 same external	13	L3
L2	L1 near10 control$4	413	L2
L1	(fabric near5 connect$3)	7295	L1

END OF SEARCH HISTORY



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	8554	fabric near5 (connect$3 or switch)	USPAT	2004/01/13 15:52			0
2	BRS	L2	965	l1 near10 control$4	USPAT	2004/01/13 15:53			0
3	BRS	L3	98	l2 same (external or remote)	USPAT	2004/01/13 15:54			0
4	BRS	L4	0	l2 same ((external or remote) adj1 (module or	USPAT	2004/01/13 15:55			0
5	BRS	L5	13	l2 same ((external or remote) near5 (module or	USPAT	2004/01/13 15:56			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6622183 B1	20030916	13	Data transmission buffer having frame counter	710/34	710/33; 710/52;
2	☐	☐	US 6542954 B1	20030401	14	Disk subsystem	710/316	710/315; 711/114
3	☐	☐	US 6498794 B1	20021224	35	Transmitter with cell switching function	370/395.1	370/466
4	☐	☐	US 6344911 B1	20020205	12	Upgradable optical communication system module	398/82	
5	☐	☐	US 6272144 B1	20010807	11	In-band device configuration protocol for ATM	370/419	
6	☐	☐	US 6259695 B1	20010710	39	Packet telephone scheduling with common time reference	370/389	370/503; 370/517
7	☐	☐	US 6151301 A	20001121	23	ATM architecture and switching element	370/232	370/414
8	☐	☐	US 6091734 A	20000718	24	Telecommunication network based on distributed control	370/410	379/229
9	☐	☐	US 5953314 A	19990914	11	Control processor switchover for a telecommunications	370/220	370/400
10	☐	☐	US 5673255 A	19970930	21	Apparatus for providing service to telephone	370/244	370/360; 370/467;
11	☐	☐	US 5583861 A	19961210	24	ATM switching element and method having independently	370/395.42	370/352; 370/395.72;

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 10 of 17 returned.

☐ 1. Document ID: US 6671819 B1

L4: Entry 1 of 17 File: USPT Dec 30, 2003

US-PAT-NO: 6671819
DOCUMENT-IDENTIFIER: US 6671819 B1

TITLE: System and methods routing packets on alterate paths

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 2. Document ID: US 6671280 B1

L4: Entry 2 of 17 File: USPT Dec 30, 2003

US-PAT-NO: 6671280
DOCUMENT-IDENTIFIER: US 6671280 B1

TITLE: Network processor for multiprotocol data flows

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 6671271 B1

L4: Entry 3 of 17 File: USPT Dec 30, 2003

US-PAT-NO: 6671271
DOCUMENT-IDENTIFIER: US 6671271 B1

TITLE: Sonet synchronous payload envelope pointer control system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 6542954 B1

L4: Entry 4 of 17 File: USPT Apr 1, 2003

US-PAT-NO: 6542954
DOCUMENT-IDENTIFIER: US 6542954 B1

h e b b g e e e f e e g ef b e

TITLE: Disk subsystem

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6535513 B1

L4: Entry 5 of 17 File: USPT Mar 18, 2003

US-PAT-NO: 6535513
DOCUMENT-IDENTIFIER: US 6535513 B1

TITLE: Multimedia and multirate switching method and apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6498794 B1

L4: Entry 6 of 17 File: USPT Dec 24, 2002

US-PAT-NO: 6498794
DOCUMENT-IDENTIFIER: US 6498794 B1

TITLE: Transmitter with cell switching function

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6430187 B1

L4: Entry 7 of 17 File: USPT Aug 6, 2002

US-PAT-NO: 6430187
DOCUMENT-IDENTIFIER: US 6430187 B1

TITLE: Partitioning of shared resources among closed user groups in a network access device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 8. Document ID: US 6359859 B1

L4: Entry 8 of 17 File: USPT Mar 19, 2002

US-PAT-NO: 6359859
DOCUMENT-IDENTIFIER: US 6359859 B1

TITLE: Architecture for a hybrid STM/ATM add-drop multiplexer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e e g ef b e

☐ 9. Document ID: US 6289015 B1

L4: Entry 9 of 17 File: USPT Sep 11, 2001

US-PAT-NO: 6289015
DOCUMENT-IDENTIFIER: US 6289015 B1

TITLE: Method and apparatus for the secure switching of a packet within a communications network

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 6272144 B1

L4: Entry 10 of 17 File: USPT Aug 7, 2001

US-PAT-NO: 6272144
DOCUMENT-IDENTIFIER: US 6272144 B1

TITLE: In-band device configuration protocol for ATM transmission convergence devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L3	17

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

h e b b g e e e f e e g ef b e

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 11 through 17 of 17 returned.

☐ 11. Document ID: US 6246680 B1

L4: Entry 11 of 17 File: USPT Jun 12, 2001

US-PAT-NO: 6246680
DOCUMENT-IDENTIFIER: US 6246680 B1

TITLE: Highly integrated multi-layer switch element architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 12. Document ID: US 6081533 A

L4: Entry 12 of 17 File: USPT Jun 27, 2000

US-PAT-NO: 6081533
DOCUMENT-IDENTIFIER: US 6081533 A

TITLE: Method and apparatus for an application interface module in a subscriber terminal unit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 13. Document ID: US 6038227 A

L4: Entry 13 of 17 File: USPT Mar 14, 2000

US-PAT-NO: 6038227
DOCUMENT-IDENTIFIER: US 6038227 A

TITLE: Preselection of service provider and functionality

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 14. Document ID: US 5953314 A

L4: Entry 14 of 17 File: USPT Sep 14, 1999

US-PAT-NO: 5953314
DOCUMENT-IDENTIFIER: US 5953314 A

h e b b cg b cc e

TITLE: Control processor switchover for a telecommunications switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 15. Document ID: US 5673255 A

L4: Entry 15 of 17 File: USPT Sep 30, 1997

US-PAT-NO: 5673255
DOCUMENT-IDENTIFIER: US 5673255 A

TITLE: Apparatus for providing service to telephone subscribers connected to a remote terminal from multiple telephone service providers

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 16. Document ID: US 5583861 A

L4: Entry 16 of 17 File: USPT Dec 10, 1996

US-PAT-NO: 5583861
DOCUMENT-IDENTIFIER: US 5583861 A

TITLE: ATM switching element and method having independently accessible cell memories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 17. Document ID: US 5375167 A

L4: Entry 17 of 17 File: USPT Dec 20, 1994

US-PAT-NO: 5375167
DOCUMENT-IDENTIFIER: US 5375167 A

TITLE: Telecommunication switching system having distributed dialing plan hierarchy

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L3	17

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Your search matched **1** of **995179** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

fabric and (connect* or switch*) and control* and (ex Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A digital read/write channel with EEPR4 detection**
Welland, D.R.; Phillip, S.M.; Leung, Ka.Y.; Tuttle, G.T.; Dupuie, S.T.; Holberg D.R.; Jack, R.V.; Sooch, N.S.; Anderson, K.D.; Armstrong, A.J.; Behrens, R.T Bliss, W.G.; Dudley, T.O.; Foland, W.R.; Glover, N.; King, L.D.;
Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC 1994 IEEE International , 16-18 Feb. 1994
Pages:276 - 277

[Abstract] [PDF Full-Text (240 KB)] **IEEE CNF**

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h eee e eee g e ch e ch e e c e e e c e

A digital read/write channel with EEPR4 detection

Welland, D.R. Phillip, S.M. Leung, Ka.Y. Tuttle, G.T. Dupuie, S.T. Holberg, D.R. Sooch, N.S. Anderson, K.D. Armstrong, A.J. Behrens, R.T. Bliss, W.G. Dudley, T. W.R. Glover, N. King, L.D.

Crystal Semicond. Corp., Austin, TX, USA;

This paper appears in: **Solid-State Circuits Conference, 1994. Digest of T Papers. 41st ISSCC., 1994 IEEE International**

Meeting Date: 02/16/1994 - 02/18/1994
Publication Date: 16-18 Feb. 1994
Location: San Francisco, CA USA
On page(s): 276 - 277
Reference Cited: 0
Inspec Accession Number: 4817620

Abstract:

This **device** increases the inter-symbol interference (ISI) manageable in a ma media read channel. It re-configures analog and digital circuits by registers tc read and write channels. The 51 mm^2 **device** is **fabricated** in a standard 0.8 poly double-metal CMOS process, and contains 128 k transistors. No **externa** components are required for operation other than standard decoupling capaci of the circuits are active while reading data from the media (data mode), and such as the use of differential analog structures, dedicated supply routes and **connections**, and shields are employed to **control** digital interference

Index Terms:

0.8 micron CMOS integrated circuits EEPR4 detection decoupling capacitors dedic routes differential analog structures digital interference digital read/write channel int interference intersymbol interference magnetic **disc** storage magnetic-media read ch analogue-digital integrated circuits single-poly double-metal CMOS process substrate **connections** 0.8 micron CMOS integrated circuits EEPR4 detection decoupling ca dedicated supply routes differential analog structures digital interference digital read/ channel inter-symbol interference intersymbol interference magnetic **disc** storage n media read channel mixed analogue-digital integrated circuits single-poly double-meta process substrate **connections**

Documents that cite this document

h eee e eee g e ch ch b c be c e ee

First Hit Fwd Refs

Generate Collection Print

L3: Entry 3 of 13 File: USPT Apr 3, 2001

DOCUMENT-IDENTIFIER: US 6210771 B1
TITLE: Electrically active textiles and articles made therefrom

Brief Summary Text (14):
In addition to serving as substrates that receive electrical components and facilitate connection therebetween, such fabric structures can be used to control external circuitry. For example, two fabric panels can be overlaid with their conductive lanes opposed and crossing at an angle, the panels being normally held apart such that compression causes electrical contact between opposed lanes. Depending on the details of implementation, this construction can serve, for example, as a switch matrix or as a touchpad that senses the physical location of a user's contact. Either of these implementations is itself suited to a wide variety of applications. A switch matrix, for example, can have a surface design assigning a unique function to each of the lane crossings (e.g., calculator numbers, musical-instrument keys, etc.), with the fabric panels connected to external (or detachable) circuitry that implements the functions in response to user interaction with the panels.

First Hit Fwd Refs

Generate Collection Print

L3: Entry 3 of 13 File: USPT Apr 3, 2001

US-PAT-NO: 6210771
DOCUMENT-IDENTIFIER: US 6210771 B1

TITLE: Electrically active textiles and articles made therefrom

DATE-ISSUED: April 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Post; E. Rehmi	Cambridge	MA		
Orth; Margaret	Cambridge	MA		
Cooper; Emily	Cambridge	MA		
Smith; Joshua R.	Cambridge	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Massachusetts Institute of Technology	Cambridge	MA			02

APPL-NO: 08/ 935466 [PALM]
DATE FILED: September 24, 1997

INT-CL: [07] B32 B 3/06, D03 D 15/00

US-CL-ISSUED: 428/100; 428/101, 428/102, 442/208, 442/209, 442/210, 2/905, 139/1R, 139/425R, 361/212
US-CL-CURRENT: 428/100; 139/1R, 139/425R, 2/905, 361/212, 428/101, 428/102, 442/208, 442/209, 442/210

FIELD-OF-SEARCH: 361/212, 139/1R, 139/425R, 2/905, 428/98, 428/99, 428/100, 428/101, 428/102, 442/31, 442/208, 442/209, 442/210, 442/902, 442/212, 442/214, 200/502, 439/67, 439/78, 439/86, 439/284, 439/285, 439/291, 439/620

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3160790	December 1964	Mittler	317/101
☐	3631298	December 1971	Davis	317/101
☐	4158103	June 1979	Danilin et al.	174/68.5
☐	4239046	December 1980	Ong	128/640

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☐	4654748	March 1987	Rees	361/220
☐	4761005	August 1988	French et al.	273/1
☐	4963768	October 1990	Agrawal et al.	307/465
☐	5499927	March 1996	Ohno et al.	439/285
☐	5774341	June 1998	Urbish et al.	361/774
☐	5802607	September 1998	Triplette	2/1
☐	5843567	December 1998	Swift et al.	428/221

OTHER PUBLICATIONS

Inaba et al., "A Full-Body Tactile Sensor Suit Using Electrically Conductive Fabric and Strings," Proc. of IROS 96 at 450 (1996).
IBM Technical Disclosure Bulletin; vol. 34 No. 7B, pp. 199-200, Dec. 1991.

ART-UNIT: 172

PRIMARY-EXAMINER: Robinson; Ellis

ASSISTANT-EXAMINER: Figueroa; John J.

ATTY-AGENT-FIRM: Cesari and McKenna, LLP

ABSTRACT:

Fabrics are used as integral elements of electrical circuitry--to facilitate control over the operation of external components connected thereto, to serve as substrates onto which electrical components are connected, or as the electrical components themselves. In one aspect, selective, anisotropic electrical conductivity is achieved using conductive fibers running along one weave direction and non-conductive fibers running along the opposite direction. The conductive fibers, which may be continuous or arranged in lanes, serve as electrical conduits capable of carrying data signals and/or power, and may be connected, for example, to electrical components soldered directly onto the fabric. In a second aspect, passive electrical components are integrated directly textiles using threads having selected electrical properties.

38 Claims, 15 Drawing figures

L3: Entry 4 of 13 File: USPT Sep 19, 2000

DOCUMENT-IDENTIFIER: US 6122253 A
TITLE: ATM network switch with congestion control

Detailed Description Text (2):
Referring first to FIG. 1, the ATM network switch illustrated is of the type described and claimed in our earlier UK Patent Application No 9507454.8, and has two switch fabrics 14a and 14b, each connected to a plurality of slot controllers 11a-f (although only six slot controllers are shown to simplify the diagram, a typical switch may have sixteen slot controllers). Each slot controller has input 12 and output 13 connections to an external data link, and includes, as may be seen from FIG. 2, a receiver 21 and a transmitter 22, either or both of which may include a buffer to control the flow of data into or out of the switch. In FIG. 2, the transmitter 22 includes a congestion control mechanism 23 controlling the storage of cells in the buffer 24. The congestion control mechanism 23 is described hereinafter in more detail with reference to FIGS. 3 and 4. Since division is more difficult to execute, the equations ##EQU3## and ##EQU4## are factored with (BS+K) to give

First Hit Fwd Refs

Generate Collection Print

L3: Entry 4 of 13 File: USPT Sep 19, 2000

US-PAT-NO: 6122253
DOCUMENT-IDENTIFIER: US 6122253 A

TITLE: ATM network switch with congestion control

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jones; Trevor	Maldon			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
General Data Comm Inc.	Waterbury	CT			02

APPL-NO: 08/ 973441 [PALM]
DATE FILED: December 4, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	9511314	June 5, 1995

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/US96/08907	June 5, 1996	WO96/39763	Dec 12, 1996	Dec 4, 1997	Dec 4, 1997

INT-CL: [07] H04 J 3/14, H04 J 3/16, H04 J 3/22, H04 J 3/24

US-CL-ISSUED: 370/235; 370/252, 370/399, 370/412, 370/129
US-CL-CURRENT: 370/235; 370/252, 370/399, 370/412

FIELD-OF-SEARCH: 370/252, 370/229, 370/230, 370/235, 370/412, 370/413, 370/414, 370/415, 370/416, 370/417, 370/418, 370/428, 370/429, 370/231, 370/232, 370/236, 370/395, 370/398, 370/399

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5550823	August 1996	Irie et al.	370/412

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☐	5787073	July 1998	Ikeda	370/236
☐	5790522	August 1998	Fichou et al.	370/236
☐	5838677	November 1998	Kozaki et al.	370/412

ART-UNIT: 271

PRIMARY-EXAMINER: Ngo; Ricky

ATTY-AGENT-FIRM: Gordon; David P. Jacobson; David S. Gallagher; Thomas A.

ABSTRACT:

An ATM network switch (11) including a buffer (24) for buffering the flow of ATM cells and a congestion control mechanism (23). The congestion control mechanism establishes a value Max, representing the maximum permissible number of ATM cells which may be stored in the buffer. The switch includes a predetermined offset value K for determining the maximum occupancy of the buffer for the connection. The congestion control mechanism determines the total number of cells TSC currently stored in the buffer and the number of cells VcCnt stored for a given connection, determines the remaining capacity BS of the buffer, calculates an adjusted value of Max as a function of TSC and BS, compares the adjusted value Max' with VcCnt, and discards the cell if VcCnt is greater than the adjusted value.

24 Claims, 5 Drawing figures

L3: Entry 5 of 13 File: USPT May 23, 2000

DOCUMENT-IDENTIFIER: US 6067286 A
TITLE: Data network switch with fault tolerance

Abstract Text (1):
An ATM data network switch having two separate but simultaneously active switch fabrics and a plurality of slot controllers is disclosed. Each slot controller has at least one external data link thereto and is separately connected to the two separate switch fabrics. Each switch fabric was the ability to switch a data cell transmitted from any one of the slot controllers to any of the other slot controllers. Each slot controller is arranged to determine the availability of the data paths to all the other slot controllers through both switch fabrics and to select for each cell to be switched a data path through one or the other of the switch fabric according to the availability determined.

Brief Summary Text (11):
In accordance with the objects of the invention, there is provided an ATM data network switch having two separate switch fabrics, and at least one switching controller, each switching controller (hereinafter referred to as "slot controller") having a plurality of external data links thereto and being separately connected to the two separate switch fabrics. Each switch fabric in turn comprises means for switching a data cell transmitted from any one of the slot controllers to any of the other slot controllers. According to the invention, both of the switch fabrics are arranged to be active at the same time and each slot controller comprises means for determining the availability of the data paths to all the other slot controllers through both switch fabrics and for selecting for each cell to be switched a data path through one or other of the switch fabrics according to the availability determined.

CLAIMS:

1. An ATM data network switch, comprising:

a) two separate switch fabrics, with both of said two separate switch fabrics being active at the same time;

b) a plurality of slot controllers, each slot controller having at least one external data link thereto and being separately connected to each of said two separate switch fabrics, wherein

each switch fabric comprising means for switching a data cell transmitted from any one of said plurality of slot controllers to any other of said plurality of slot controllers, and

each of said plurality of slot controller comprises (i) means for determining the availability of data paths to all others of said plurality of slot controllers through both said two separate switch fabrics, (ii) means for storing an indicator of the availability of each of the data paths from and to the said slot controller, said means for storing being coupled to said means for determining and (iii) means for selecting, for each cell to be switched, a data path through one or other of two separate switch fabrics and for sending the cell via said data path according

to the availability determined by said means for determining and stored in said means for storing, said means for selecting being coupled to said means for storing.

h e b b cg b cc e

L3: Entry 5 of 13 File: USPT May 23, 2000

DOCUMENT-IDENTIFIER: US 6067286 A
TITLE: Data network switch with fault tolerance

Abstract Text (1):
An ATM data network switch having two separate but simultaneously active switch fabrics and a plurality of slot controllers is disclosed. Each slot controller has at least one external data link thereto and is separately connected to the two separate switch fabrics. Each switch fabric was the ability to switch a data cell transmitted from any one of the slot controllers to any of the other slot controllers. Each slot controller is arranged to determine the availability of the data paths to all the other slot controllers through both switch fabrics and to select for each cell to be switched a data path through one or the other of the switch fabric according to the availability determined.

Brief Summary Text (11):
In accordance with the objects of the invention, there is provided an ATM data network switch having two separate switch fabrics, and at least one switching controller, each switching controller (hereinafter referred to as "slot controller") having a plurality of external data links thereto and being separately connected to the two separate switch fabrics. Each switch fabric in turn comprises means for switching a data cell transmitted from any one of the slot controllers to any of the other slot controllers. According to the invention, both of the switch fabrics are arranged to be active at the same time and each slot controller comprises means for determining the availability of the data paths to all the other slot controllers through both switch fabrics and for selecting for each cell to be switched a data path through one or other of the switch fabrics according to the availability determined.

CLAIMS:

1. An ATM data network switch, comprising:

a) two separate switch fabrics, with both of said two separate switch fabrics being active at the same time;

b) a plurality of slot controllers, each slot controller having at least one external data link thereto and being separately connected to each of said two separate switch fabrics, wherein

each switch fabric comprising means for switching a data cell transmitted from any one of said plurality of slot controllers to any other of said plurality of slot controllers, and

each of said plurality of slot controller comprises (i) means for determining the availability of data paths to all others of said plurality of slot controllers through both said two separate switch fabrics, (ii) means for storing an indicator of the availability of each of the data paths from and to the said slot controller, said means for storing being coupled to said means for determining and (iii) means for selecting, for each cell to be switched, a data path through one or other of two separate switch fabrics and for sending the cell via said data path according

to the availability determined by said means for determining and stored in said means for storing, said means for selecting being coupled to said means for storing.

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L3: Entry 5 of 13 File: USPT May 23, 2000

US-PAT-NO: 6067286
DOCUMENT-IDENTIFIER: US 6067286 A

TITLE: Data network switch with fault tolerance

DATE-ISSUED: May 23, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jones; Trevor	Maldon			GB
Barnett; Richard	Maldon			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
General DataComm, Inc.	Middlebury	CT			02

APPL-NO: 08/ 930973 [PALM]
DATE FILED: October 7, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	9507454	April 11, 1995

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/US96/05029	April 9, 1996	WO96/32790	Oct 17, 1996	Oct 7, 1997	Oct 7, 1997

INT-CL: [07] H04 L 12/26

US-CL-ISSUED: 370/218; 370/244, 370/248
US-CL-CURRENT: 370/218; 370/244, 370/248

FIELD-OF-SEARCH: 370/216, 370/217, 370/218, 370/219, 370/220, 370/221, 370/222, 370/225, 370/227, 370/228, 370/242, 370/244, 370/248, 370/250, 370/251, 370/360, 370/386, 370/387, 370/388

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

h e b b g e e e f c e b e ge

☐	5179552	January 1993	Chao	370/389
☐	5485453	January 1996	Wahlman et al.	370/217
☐	5550815	August 1996	Cloonan et al.	370/396
☐	5574718	November 1996	Eckhoff et al.	370/228
☐	5724352	March 1998	Cloonan et al.	370/395
☐	5740157	April 1998	Demiray et al.	370/219

ART-UNIT: 271

PRIMARY-EXAMINER: Pham; Chi H.

ASSISTANT-EXAMINER: Yao; Kwang B.

ATTY-AGENT-FIRM: Gordon; David P. Jacobson; David S. Gallagher; Thomas A.

ABSTRACT:

An ATM data network switch having two separate but simultaneously active switch fabrics and a plurality of slot controllers is disclosed. Each slot controller has at least one external data link thereto and is separately connected to the two separate switch fabrics. Each switch fabric was the ability to switch a data cell transmitted from any one of the slot controllers to any of the other slot controllers. Each slot controller is arranged to determine the availability of the data paths to all the other slot controllers through both switch fabrics and to select for each cell to be switched a data path through one or the other of the switch fabric according to the availability determined.

20 Claims, 9 Drawing figures

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L3: Entry 6 of 13 File: USPT Nov 23, 1999

DOCUMENT-IDENTIFIER: US 5991295 A
TITLE: Digital switch

Detailed Description Text (14):
The switch fabric data controller ASIC 6 connects to the external shared memory 8 by means of a quarter cell width data bus 17. Whole cells are written to or read from the shared memory 8 on the databus 17 in four 20 nanosecond cycles. This is described in detail below.

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L3: Entry 6 of 13 File: USPT Nov 23, 1999

US-PAT-NO: 5991295
DOCUMENT-IDENTIFIER: US 5991295 A

TITLE: Digital switch

DATE-ISSUED: November 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tout; Arthur James Viggo	Berkshire			GB
Johnson; Stephen Mark	Bucks			GB

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Madge Networks Limited	Buckinghamshire			GB	03

APPL-NO: 08/ 729755 [PALM]
DATE FILED: October 7, 1996

PARENT-CASE:
The present application claims the benefit of Provisional Application No. 60/007,542, filed Nov. 24, 1995.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
GB	9520686	October 10, 1995

INT-CL: [06] H04 L 12/56

US-CL-ISSUED: 370/376; 370/395
US-CL-CURRENT: 370/395.7; 370/395.72

FIELD-OF-SEARCH: 370/237, 370/428, 370/429, 370/412, 370/415, 370/416, 370/410, 370/468, 370/418, 370/414, 370/229, 370/375, 370/376, 370/395

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5132966	July 1992	Hayano et al.	370/468

h e b b g e e e f c e b e ge

☐	5452330	September 1995	Goldstein	375/257
☐	5521913	May 1996	Gridley et al.	370/428
☐	5570355	October 1996	Dail et al.	370/352
☐	5640387	June 1997	Takahashi et al.	370/359

ART-UNIT: 275

PRIMARY-EXAMINER: Horabik; Michael

ASSISTANT-EXAMINER: Harper; Kevin C.

ATTY-AGENT-FIRM: Sughrue, Mion, Zinn, Macpeak & Seas, PLLC

ABSTRACT:

A switch fabric is provided which comprises a shared memory, a number of switch fabric ports, and a switch fabric data controller. The switch fabric data controller routes blocks of data received at one switch fabric port to one or more other switch fabric ports and writes and reads data to and from, respectively, the shared memory. The switch fabric data controller preferentially routes a block of data from the one switch fabric port to the one or more other switch fabric ports without writing the block of data into the shared memory if the one or more other desired switch fabric ports are free or become free within a predetermined period, and otherwise writes the block of data into the shared memory for temporary storage if the one or more other switch fabric ports are busy. In this manner, the switch fabric facilitates "cut-through" of blocks of data across a switch without the need to write the blocks of data to a shared memory, thereby reducing latency.

17 Claims, 8 Drawing figures

L3: Entry 7 of 13 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5777994 A
TITLE: ATM switch and intermediate system

Brief Summary Text (17):
In one preferred aspect, an ATM switch according to the present invention provides an interconnection between a connection-oriented ATM LAN of an ATM system and a connectionless legacy LAN. The ATM switch comprises a management and control block for managing and controlling operations for electrical connections between networks, a segmentation and reassembly block for providing an interchange between each cell transmitted over the ATM LAN and a packet transmitted over the legacy LAN, an ATM switch or switch fabric, a legacy LAN interface with bridging/routing processor for providing an electrical connection to the legacy LAN, an ATM interface with bridging/routing processor for providing an electrical connection to the ATM LAN and at least one ATM interface. The management and control block, the legacy LAN interface with bridging/routing processor and the ATM interface with bridging/routing processor are electrically connected to one another via a bus. An external interface of the legacy LAN interface with bridging/routing processor is electrically connected to the legacy LAN. The management and control block and one port of the switch fabric are electrically connected to each other through the segmentation and reassembly block interposed therebetween. Further, an external interface of the ATM interface with bridging/routing processor and one port of the switch fabric are electrically connected to each other through the ATM interface. Ports other than the above ports of the switch fabric are connected to the ATM LAN through the ATM interface.

Brief Summary Text (21):
Further, an intermediate system according to the present invention comprises a switch fabric electrically connected to an ATM LAN indicative of a connection-oriented network through at least one ATM interface, a management and control block electrically connected to one port of the switch fabric through a segmentation and reassembly block, a first bridging processor electrically connected to the management and control block through a bus line and having an external interface to which a legacy LAN indicative of a connectionless network is connected, and a second bridging processor electrically connected to the management and control block through the bus line and having an external interface electrically connected to one port of the switch fabric through the segmentation and reassembly block.

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L3: Entry 7 of 13 File: USPT Jul 7, 1998

US-PAT-NO: 5777994
DOCUMENT-IDENTIFIER: US 5777994 A

TITLE: ATM switch and intermediate system

DATE-ISSUED: July 7, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Takihiro; Masatoshi	Fujisawa			JP
Murakami; Toshihiko	Fujisawa			JP
Fukushima; Hidehiro	Fujisawa			JP
Takada; Osamu	Sagamihara			JP
Kimoto; Atsushi	Hadano			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 601354 [PALM]
DATE FILED: February 16, 1996

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	7-053289	February 17, 1995

INT-CL: [06] H04 L 12/56

US-CL-ISSUED: 370/395; 370/401
US-CL-CURRENT: 370/395.53; 370/401

FIELD-OF-SEARCH: 370/352, 370/353, 370/354, 370/356, 370/355, 370/389, 370/394, 370/395, 370/396, 370/402, 370/428, 370/392, 370/397, 370/400, 370/401, 370/403, 370/404, 370/408, 370/320

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5379297	January 1995	Glover et al.	370/355

h e b b g e e e f c e b e ge

☐	5408469	April 1995	Opher et al.	370/474
☐	5450411	September 1995	Heil	370/419

ART-UNIT: 263

PRIMARY-EXAMINER: Ton; Dang

ATTY-AGENT-FIRM: Antonelli, Terry, Stout, & Kraus, LLP

ABSTRACT:

An ATM switch for providing an electrical interconnection between a connection-oriented ATM LAN of an ATM system and a connectionless legacy LAN is provided. The ATM switch includes a switch fabric electrically connected to the ATM LAN, a segmentation and reassembly block electrically connected to the switch fabric, for providing an interchange between one of cells transmitted over the ATM LAN and a packet transmitted over the legacy LAN, a management and control block electrically connected to the switch fabric through the segmentation and control block so as to manage and control operations for electrical connections between networks, a first bridging/routing processor having a legacy LAN interface for providing electrical connections between the legacy LAN and the first bridging/routing processor, a second bridging/routing processor electrically connected to the switch fabric through at least one ATM interface, and a bus for providing electrical connections between the management and control block, the first bridging/routing processor and the second bridging/routing processor. A LAN emulation configuration server function for managing configurations of a plurality of virtual LAN segments on the ATM LAN, which are required upon LAN emulation, a LAN emulation server function for obtaining an address resolution to an ATM address from a media access address, and a broadcast and unknown server function for making a broadcast to a terminal in the LAN are provided so as to be distributed to the management and control block or the second bridging/routing processor.

11 Claims, 11 Drawing figures

L3: Entry 9 of 13 File: USPT Mar 7, 1995

DOCUMENT-IDENTIFIER: US 5396491 A
TITLE: Self-routing switching element and fast packet switch

Detailed Description Text (26):
In FIG. 2, the packet signals on input port 2-0 typically connect through an input buffer 23 to the input controller 6-0. Input buffer 23 is optionally part of the input controller 6-0 or may be external to the controller. In one embodiment, input buffer 23 is a first-in-first-out (FIFO) buffer which receives a plurality of input packet signals which are intended for distribution to particular ones of the output controllers 7 of FIG. 1. The packet signals input from the port 2-0 have tags which specify, among other things, a particular one of the output ports 3 as connected through the switch path fabric 8 and a particular one of the output controllers 7. The switch fabric 8, in response to the tags of packets signals input to the controllers 6 of FIG. 1 and specifically the input controller 6-0 of FIG. 2, transmits the input packet signals to a particular one of the output port controllers 7 and the corresponding output port 3.

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L3: Entry 12 of 13 File: USPT Jun 22, 1993

DOCUMENT-IDENTIFIER: US 5222085 A
TITLE: Self-routing switching element and fast packet switch

Detailed Description Text (26):
In FIG. 2, the packet signals on input port 2-0 typically connect through an input buffer 23 to the input controller 6-0. Input buffer 23 is optionally part of the input controller 6-0 or may be external to the controller. In one embodiment, input buffer 23 is a first-in-first-out (FIFO) buffer which receives a plurality of input packet signals which are intended for distribution to particular ones of the output controllers 7 of FIG. The packet signals input from the port 2-0 have tags which specify, among other things, a particular one of the output ports 3 as connected through the switch path fabric 8 and a particular one of the output controllers 7. The switch fabric 8, in response to the tags of packets signals input to the controllers 6 of FIG. 1 and specifically the input controller 6-0 of FIG. 2, transmits the input packet signals to a particular one of the output port controllers 7 and the corresponding output port 3.

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L3: Entry 12 of 13 File: USPT Jun 22, 1993

US-PAT-NO: 5222085
DOCUMENT-IDENTIFIER: US 5222085 A

TITLE: Self-routing switching element and fast packet switch

DATE-ISSUED: June 22, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Newman; Peter	Mountain View	CA	94043	

APPL-NO: 07/ 602409 [PALM]
DATE FILED: October 22, 1990

PARENT-CASE:
This application is a continuation-in-part of the above-identified cross-referenced applications Ser. No. 07/258,291, filed 10/14/88, now U.S. Pat. No. 4,965,788 and U.S. Pat. No. 07/582,254, filed 09/14/90, now abandoned.

INT-CL: [05] H04Q 11/04, H04J 3/24

US-CL-ISSUED: 370/60; 370/94.1
US-CL-CURRENT: 370/422

FIELD-OF-SEARCH: 370/58.1, 370/58.2, 370/58.3, 370/60, 370/60.1, 370/85.1, 370/94.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4482996	November 1984	Wilson et al.	370/60
☐	4488151	December 1984	Bolton et al.	370/85.1
☐	4621359	November 1986	McMillen	370/94.1
☐	4630260	December 1986	Toy et al.	370/94.1
☐	4661947	April 1987	Lea et al.	370/94.1
☐	4707831	November 1987	Weir et al.	370/94.1
☐	4731878	March 1988	Vaidya	370/60
☐	4734907	March 1988	Turner	370/94.1

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☐	4764919	August 1988	Hunter et al.	370/60

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
2151880	July 1985	GB	

OTHER PUBLICATIONS

"Binary Routing Networks", Milway D. R., U. of Cambridge Computer Lab, Tech. Report No. 101, Cambridge, England, Dec. 1986 (Entire document).

ART-UNIT: 263

PRIMARY-EXAMINER: Olms; Douglas W.

ASSISTANT-EXAMINER: Hsu; Alpus H.

ABSTRACT:

A self-routing switching element in a packet switch functions in a packet synchronous mode in which a plurality of the incoming packet signals are switched by the switching element concurrently during a common time period. For each incoming packet signal received during the common time period, the switching element detects that one of the inputs has an incoming packet signal for transmission to one of the outputs, determines if the one of the output modules will accept the incoming packet signals, and responsive to the determination, enables the acceptance of the incoming packet signal by the output module for transmission to the output. The control circuitry is distributed throughout the switching element in output modules, one module for each output from the switching element.

2 Claims, 17 Drawing figures

L5: Entry 3 of 17 File: USPT Apr 1, 2003

DOCUMENT-IDENTIFIER: US 6542954 B1
TITLE: Disk subsystem

Detailed Description Text (3):
In the external storage device shown in the figure, N disk array controllers (controller section) 1-1 to 1-N (controllers in middle such as 1-2 are not shown, this applies to hereinbelow) are connected to a host computer (not shown) in an upper side, and provide M disk drive interface (disk drive I/F) controllers 2-1 to 2-M in a bottom side. The hardware configuration of the disk array controller will be described below in greater details. Each of M controllers of fibre channel fabric switch 3-1 to 3-M are respectively connected to the disk drive interface (I/F) controllers 2-1 to 2-M for controlling disk drive units through their fibre channel interface 5. L disk drive units are connected to one fibre channel fabric switch controller, a total of M by L disk drive units (4(1,1) to 4(M,L)) are connected to the fibre channel fabric switch controllers 3-1 to 3-M through fibre channel interfaces 6.

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L5: Entry 3 of 17 File: USPT Apr 1, 2003

US-PAT-NO: 6542954
DOCUMENT-IDENTIFIER: US 6542954 B1

TITLE: Disk subsystem

DATE-ISSUED: April 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Aruga; Kazuhisa	Odawara			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 09/ 495868 [PALM]
DATE FILED: February 2, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	11-024648	February 2, 1999

INT-CL: [07] G06 F 13/16, G06 F 13/42

US-CL-ISSUED: 710/316; 710/315, 711/114
US-CL-CURRENT: 710/316; 710/315, 711/114

FIELD-OF-SEARCH: 711/114, 711/111, 711/112, 714/5, 714/6, 714/7, 710/11, 710/62, 710/65, 710/74, 710/38, 710/315, 710/316

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5077736	December 1991	Dunphy, Jr. et al.	714/7
☐	5274645	December 1993	Idleman et al.	714/6
☐	5471586	November 1995	Sefidvash et al.	710/104
☐	5699533	December 1997	Sakai	710/316
☐	5729763	March 1998	Leshem	710/38

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☐	5768551	June 1998	Bleiweiss et al.	710/316
☐	5867640	February 1999	Aguilar et al.	714/6
☐	6148414	November 2000	Brown et al.	714/9
☐	6185203	February 2001	Berman	370/351
☐	6247077	June 2001	Muller et al.	710/74
☐	6324181	November 2001	Wong et al.	370/403

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
10171746	June 1998	JP	

ART-UNIT: 2187

PRIMARY-EXAMINER: Portka; Gary J.

ATTY-AGENT-FIRM: Antonelli, Terry, Stout & Kraus, LLP

ABSTRACT:

A protocol controller disposed between switches in a fiber channel fabric switch circuit and disk drive units for converting a protocol to enable one-to-one connectivity established between controllers and disk drive units.

35 Claims, 7 Drawing figures

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L5: Entry 7 of 17 File: USPT Sep 11, 2001

DOCUMENT-IDENTIFIER: US 6289015 B1
TITLE: Method and apparatus for the secure switching of a packet within a communications network

Detailed Description Text (10):
FIG. 4 is a block diagram illustrating an exemplary implementation of the switch 60, shown in FIG. 3. A switch core 80 (a.k.a. a switching fabric) is shown to include the ports 62 and 64, an array of corresponding Media Access Control (MAC) ports 82 and an External Address Match (EAM) interface 84. An external physical layer device (PHY) 66 is coupled to each port. Each of the PHYs 66 may be a 10 BaseT PHY, or a specialized PHY to facilitate communications over the POTS wiring 20. In one exemplary embodiment, such a specialized PHY may comprise the HomeRun PHY, developed by Tut Systems, Inc. of Pleasant Hill, Calif. The switch core 80 also includes a data path, switching logic, internal single-address compare, and network statistics logic (all not shown).

First Hit Fwd Refs

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L5: Entry 7 of 17 File: USPT Sep 11, 2001

US-PAT-NO: 6289015
DOCUMENT-IDENTIFIER: US 6289015 B1

TITLE: Method and apparatus for the secure switching of a packet within a communications network

DATE-ISSUED: September 11, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Warner; Thomas E.	Moraga	CA		
Corder; Patrick L.	Martinez	CA		
Miller; Mark S.	Oakland	CA		
Ethier; Steven L.	Pleasanton	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Tut Systems, Inc.	Pleasant Hill	CA			02

APPL-NO: 09/ 156570 [PALM]
DATE FILED: September 17, 1998

INT-CL: [07] H04 L 12/28

US-CL-ISSUED: 370/392; 370/352, 370/389
US-CL-CURRENT: 370/392; 370/352, 370/389

FIELD-OF-SEARCH: 370/351, 370/389, 370/396, 370/398, 370/400, 370/422, 370/535, 370/537, 370/902, 370/352

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5689644	November 1997	Cou et al.	370/392
☐	6009092	December 1999	Basilico	370/352
☐	6084878	July 2000	Crayford et al.	370/389

OTHER PUBLICATIONS

h e b b g e e e f c e c e ge

"TNETX-15AE Address-Lookup Device", Texas Instruments Datasheets, pp1-78, SPWS041A, Aug. 1997, revised Oct. 1997.
"TNETX3100--ThunderSwitch.TM. 10-Port 10-/100-MBIT/S Ethernet.TM. Switch", Texas Instruments Datasheets, pp 1-79, SPWS031D, Jun. 1997, revised Oct. 1997.
"TNETX3150/TNETX3150A ThunderSwitch.TM. 15-Port 10-/100-MBIT/S Ethernet.TM. Switch", Texas Instruments Database, pp 1-112, SPWS027F, Feb. 1997, revised Sep. 1997.

ART-UNIT: 262

PRIMARY-EXAMINER: Olms; Douglas

ASSISTANT-EXAMINER: Mehra; Indes Pal

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A switch for switching a packet within a communications network includes a switching core that services a number of ports. The switch also includes address matching logic, coupled to the switching core, that implements an address lookup scheme according to which the switching core may switch to packet received at the switch. Override logic, that is also coupled to the switching core, determines with a packet received at any one of the number of ports serviced by the switching core is received at a predetermined port. This may be done by snooping a bus within the switch that provides an indication of an active port. If the packet was not received at the predetermined port, the override logic override the address matching logic to cause the switching core to route the packet exclusively to the first port.

42 Claims, 6 Drawing figures

L5: Entry 10 of 17 File: USPT Nov 21, 2000

DOCUMENT-IDENTIFIER: US 6151301 A
TITLE: ATM architecture and switching element

Detailed Description Text (8):
FIG. 4 is a block diagram of a routing table circuit 42 according to the present invention. The routing table circuit 42 is a combination storage and control device that is used with external memory, e.g., SRAM 90, and includes a receive queue controller 80 which sends data to the switch fabric and receives a back-pressure signal from the switch fabric, and a transmission buffer controller 82 which receives data from the switch fabric after that data has been processed by the multicast header translation circuit 84 and asserts back pressure to the switch fabric. The transmission buffer controller 82 also includes a small buffer memory 86 for storing cells received from the switch fabric. A further controller, called a connection table controller 88, is for reading header information from the workstation interface and is operative to use that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Controller 88 stores information about switch tags and buffers data in external SRAM 90. Further included are an interrupt processor 92 and processor interface 94, which are for sending control signals. to the workstation. Optionally included is an OAM/BECN cell transmit circuit 96 for inserting control cells to the outgoing data stream.

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L5: Entry 10 of 17 File: USPT Nov 21, 2000

US-PAT-NO: 6151301
DOCUMENT-IDENTIFIER: US 6151301 A

TITLE: ATM architecture and switching element

DATE-ISSUED: November 21, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holden; Brian D.	Sunnyvale	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PMC-Sierra, Inc.	Burnaby			CA	03

APPL-NO: 08/ 680869 [PALM]
DATE FILED: July 16, 1996

PARENT-CASE:
This is a continuation of application No. 08/439,078 filed May 11, 1995, now U.S. Pat. No. 5,570,348.

INT-CL: [07] G06 F 11/00, H04 L 12/28

US-CL-ISSUED: 370/232; 370/395, 370/414
US-CL-CURRENT: 370/232; 370/414

FIELD-OF-SEARCH: 370/229, 370/230, 370/232, 370/235, 370/236, 370/412, 370/413-418, 370/395

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5083269	January 1992	Syobatake et al.	370/85.6 X
☐	5099475	March 1992	Kozaki et al.	370/60
☐	5144619	September 1992	Munter	370/60.1
☐	5233606	August 1993	Pashan et al.	370/418
☐	5280470	January 1994	Buhrke et al.	370/232

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☐	5285444	February 1994	Sakurai et al.	370/60
☐	5313454	May 1994	Bustini et al.	370/236
☐	5317561	May 1994	Fischer et al.	370/60.1 X
☐	5325356	June 1994	Lyles	370/60
☐	5367520	November 1994	Cordell	370/395
☐	5493566	February 1996	Ljungberg et al.	370/395
☐	5570348	October 1996	Holden	370/236

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Alles, "Tutorial: ATM in Private Networking,"Hughes LAN Systems, 1993.
Chen, et al., "Performance Sutdy of an Input Queuing Packet Switch with Two Priority cases," IEEE Trans. Commun., pp. 117-126, Jan. 1991, reprinted in Performance Evaluation, pp. 99-107.
Fujitsu (pub.), Asynchronous Transfer Mode: IC's for ATM, 1993.
IEEE Press (pub.), Performance Evaluation of High Speed Switching Fabrics and Networks, Robertazzi (ed.), pp. 1-3, 251-252, 1993.
Karol, et al., "Input Versus Output Queuing on a Space Division Packet Switch," IEEE Trans. Commun., pp.1347-1356, Dec. 1987, reprinted in Performance Evaluation, pp. 59-68.
Kim, et al., "Call Scheduling Algorithms in a Multicast Switch," IEEE Trans. Commun., pp. 625-635, Mar. 1992, reprinted in Performance Evaluation, pp. 290-299.

ART-UNIT: 279

PRIMARY-EXAMINER: Nguyen; Chau

ASSISTANT-EXAMINER: Nguyen; Phuongchau Ba

ATTY-AGENT-FIRM: Townsend & Townsend and Crew LLP Allen; Kenneth R.

ABSTRACT:

An ATM switching system architecture of a switch fabric-type is built of, a plurality of ATM switch element circuits and routing table circuits for each physical connection to/from the switch fabric. A shared pool of memory is employed to eliminate the need to provide memory at every crosspoint. Each routing table maintains a marked interrupt linked list for storing information about which ones of its virtual channels are experiencing congestion. This linked list is available to a processor in the external workstation to alert the processor when a congestion condition exists in one of the virtual channels. The switch element circuit typically has up to eight 4-bit-wide nibble inputs and eight 4-bit-wide nibble outputs and is capable of connecting cells received at any of its inputs to any of its outputs, based on the information in a routing tag uniquely associated with each cell.

4 Claims, 17 Drawing figures

L5: Entry 11 of 17 File: USPT Jul 18, 2000

DOCUMENT-IDENTIFIER: US 6091734 A
TITLE: Telecommunication network based on distributed control

Brief Summary Text (17):
On the other hand, under remote control, in other words when the controller and the switch fabric devices are remotely located as shown in FIG. 3, in the send mode, a drive order 43 is basically sent by an input/output channel command. That is, the central controller 11 of the central office 10 executes an input-output instruction (SIO instruction) 40 and activates the channel multiplexer 13. The channel multiplexer 13 sequentially reads a command address word (CAW) 41 and a channel command (CCW) 42 from the main memory 12, and activates the general subchannel 14-1. The general subchannel 14-1 reads the switch fabric drive order 43 from the area in the main memory 12 designated by the CCW 42 and sends the switch fabric drive order 43 to the remote controller 15. The remote controller 15 sends the drive order 43 to the remote office data sender-receiver 21 via the control information link 16-1. The remote office data sender-receiver 21 transfers the drive order 43 to the switch controller 24, the switch controller 24 checks and interprets the drive order 43, and the switch fabric 23 is made to perform the desired switching operation. Once the switching operation is completed, the remote office data sender-receiver 21 returns an execution completion signal to the remote controller 15 via the control information link 16-1. When the remote controller 15 sends an execution completion signal to the general subchannel 14-1, the channel multiplexer 13 causes an interrupt to the central controller 11. The central controller 11 analyzes the cause of the interrupt to find that the execution of the switch fabric drive order has been completed. The designation of which of the plurality of remote offices 20 are to be controlled is done by the channel number field of the channel instruction 40. Thus, a single central office 10 is capable of transferring control information between a plurality of remote offices 20 by using sets of CAW 41, CCW 42 and switch fabric drive order 43 which are different for each channel number.

Brief Summary Text (23):
The above mentioned remote control switching system is considered as one type of the distributed switching system and the other type of distributed switching system is a LAN(Local Area Network)-based distributed switching system in which the controller and the switch fabric devices are connected not by dedicated lines as in a remote control switching system, but instead are connected by a LAN (Local Area Network) has been proposed. In this distributed switching system, call connection control is performed under the cooperation of the controller (central processing-management module) and the switch fabric devices (switching modules) by sending and receiving through a LAN (Japanese Patent Application, First Publication No. Sho 62-188590).

Brief Summary Text (27):
(3) Additionally, the communication means or methods for the case of direct control in which the controller and the switch fabric devices are in the same node and the case of remote control in which the controller and the switch fabric devices are located remotely are different, so that the application program must include separate codes for direct control and remote control. This courses high development cost and low flexibility.

Brief Summary Text (34):
The object of the present invention is to offer a telecommunication network based on distributed control which resolves such conventional problems, with flexibility such as to allow arbitrary control nodes and switch nodes to be flexibly connected, with low communication overhead between the controller and the switch fabric devices, and wherein the decrease in performance is small in the case of remote control even if the distance between the control nodes and the switch nodes is large.

First Hit Fwd Refs

Generate Collection Print

L5: Entry 11 of 17 File: USPT Jul 18, 2000

US-PAT-NO: 6091734
DOCUMENT-IDENTIFIER: US 6091734 A

TITLE: Telecommunication network based on distributed control

DATE-ISSUED: July 18, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Suzuki; Shigehiko	Tokyo			JP
Yamada; Shigeki	Tokorozawa			JP
Kubota; Minoru	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Nippon Telegraph and Telephone Corporation				JP	03

APPL-NO: 08/ 933783 [PALM]
DATE FILED: September 19, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-249985	September 20, 1996

INT-CL: [07] H04 M 7/00, H04 M 1/66, H04 M 1/68, H04 M 3/16

US-CL-ISSUED: 370/410; 379/229
US-CL-CURRENT: 370/410; 379/229

FIELD-OF-SEARCH: 370/389, 370/395, 370/396, 370/397, 370/401, 370/399, 370/400, 370/410, 370/352, 370/353, 370/354, 379/219, 379/220, 379/229, 379/230, 379/231, 379/232, 379/234, 379/240

PRIOR-ART-DISCLOSED:

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☐	5388096	February 1995	Westberg	370/375
☐	5488501	January 1996	Barnsley	359/137

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☐	5509123	April 1996	Dobbins et al.	370/389
☐	5848128	December 1998	Frey	379/230
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☐	5940491	August 1999	Anderson et al.	379/230

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5-268254	October 1993	JP	

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Shimizu et al., "Low Latency Message Communication Support for the AP1000," PIOC 19th International Symposium on Computer Architecture, 1992, pp. 288-297 No Month.
Kogiku et al., "Distributed Object-Oriented Network Architecture DONA: Design Concepts," Information and Communication Engineers, Mar. 27, 1996.
Suzuki et al., "DONA: A Distributed Object-Oriented Network Architecture," The Institute of Electronics, Information and Communication Engineers, Technical Report of IEICE, Sep. 24, 1996, pp. 25-30.

ART-UNIT: 275

PRIMARY-EXAMINER: Vu; Huy D.

ASSISTANT-EXAMINER: Harper; Kevin C.

ATTY-AGENT-FIRM: Pennie & Edmonds LLP

ABSTRACT:

A telecommunication network based on distributed control, comprising a plurality of switch nodes having switch fabric devices containing switches for exchanging user information between subscriber lines and trunk lines, and signal devices for sending and receiving control signals through the subscriber lines and the trunk lines; a plurality of control nodes for controlling the switch nodes by sending and receiving control messages with the switch nodes; a control network for performing mutual message communications between the switch nodes and the control nodes; and an user information network for transferring the user information; wherein the control network connects the switch nodes and the control nodes by connection-type or connectionless communications, the control nodes and the switch nodes send and receive messages for communicating with other nodes through the control network, and each of the control nodes controls a plurality of switch nodes based on the control network routing messages to specified destination nodes in accordance with routing information in the messages.

11 Claims, 13 Drawing figures

First Hit Fwd Refs

End of Result Set

☐ Generate Collection Print

L5: Entry 17 of 17 File: USPT Sep 17, 1996

DOCUMENT-IDENTIFIER: US 5557607 A
TITLE: Methods and apparatus for enqueueing and dequeueing data cells in an ATM switch fabric architecture

Detailed Description Text (8):
FIG. 4 is a block diagram of a routing table circuit 42 according to the present invention. The routing table circuit 42 is a combination storage and control device that is used with external memory, e.g., SRAM 90, and includes a receive queue controller 80 which sends data to the switch fabric and receives a back-pressure signal from the switch fabric, and a transmission buffer controller 82 which receives data from the switch fabric after that data has been processed by the multicast header translation circuit 84 and asserts back pressure to the switch fabric. The transmission buffer controller 82 also includes a small buffer memory 86 for storing cells received from the switch fabric. A further controller, called a connection table controller 88, is for reading header information from the workstation interface and is operative to use that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Controller 88 stores information about switch tags and buffers data in external SRAM 90. Further included are an interrupt processor 92 and processor interface 94, which are for sending control signals to the workstation. Optionally included is an OAM/BECN cell transmit circuit 96 for inserting control cells to the outgoing data stream.

US-PAT-NO: 6542954

DOCUMENT-IDENTIFIER: US 6542954 B1

TITLE: Disk subsystem

---------- KWIC ---------

Detailed Description Text - DETX (3):

In the external storage device shown in the figure, N disk array controllers (controller section) 1-1 to 1-N (controllers in middle such as 1-2 are not shown, this applies to hereinbelow) are connected to a host computer (not shown) in an upper side, and provide M disk drive interface (disk drive I/F) controllers 2-1 to 2-M in a bottom side. The hardware configuration of the disk array controller will be described below in greater details. Each of M controllers of fibre channel fabric switch 3-1 to 3-M are respectively connected to the disk drive interface (I/F) controllers 2-1 to 2-M for controlling disk drive units through their fibre channel interface 5. L disk drive units are connected to one fibre channel fabric switch controller, a total of M by L disk drive units (4(1,1) to 4(M,L)) are connected to the fibre channel fabric switch controllers 3-1 to 3-M through fibre channel interfaces 6.

US006542954B1

(12) **United States Patent**
Aruga

(10) **Patent No.: US 6,542,954 B1**
(45) **Date of Patent: Apr. 1, 2003**

(54) **DISK SUBSYSTEM**

(75) Inventor: **Kazuhisa Aruga**, Odawara (JP)

(73) Assignee: **Hitachi, Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/495,868**

(22) Filed: **Feb. 2, 2000**

(30) **Foreign Application Priority Data**

Feb. 2, 1999 (JP) 11-024648

(51) **Int. Cl.**[7] **G06F 13/16**; G06F 13/42
(52) **U.S. Cl.** **710/316**; 710/315; 711/114
(58) **Field of Search** 711/114, 111, 112; 714/5, 6, 7; 710/11, 62, 65, 74, 36, 315, 316

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5,867,640 A * 2/1999 Aguilar et al. 714/6
6,148,414 A 11/2000 Brown et al. 714/9
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6,247,077 B1 * 6/2001 Muller et al. 710/74
6,324,181 B1 * 11/2001 Wong et al. 370/403

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JP 10171746 6/1998

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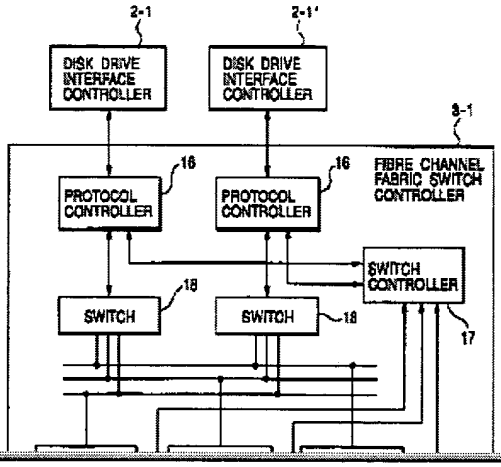
Primary Examiner—Gary J. Portka
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP

(57) **ABSTRACT**

A protocol controller disposed between switches in a fiber channel fabric switch circuit and disk drive units for converting a protocol to enable one-to-one connectivity established between controllers and disk drive units.

35 Claims, 7 Drawing Sheets



US-PAT-NO: 6151301

DOCUMENT-IDENTIFIER: US 6151301 A

TITLE: ATM architecture and switching element

---------- KWIC ---------

Detailed Description Text - DETX (8):

FIG. 4 is a block diagram of a routing table circuit 42 according to the present invention. The routing table circuit 42 is a combination storage and control device that is used with external memory, e.g., SRAM 90, and includes a receive queue controller 80 which sends data to the switch fabric and receives a back-pressure signal from the switch fabric, and a transmission buffer controller 82 which receives data from the switch fabric after that data has been processed by the multicast header translation circuit 84 and asserts back pressure to the switch fabric. The transmission buffer controller 82 also includes a small buffer memory 86 for storing cells received from the switch fabric. A further controller, called a connection table controller 88, is for reading header information from the workstation interface and is operative to use that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Controller 88 stores information about switch tags and buffers data in external SRAM 90. Further included are an interrupt processor 92 and processor interface 94, which are for sending control signals. to the workstation. Optionally included is an OAM/BECN cell transmit circuit 96 for inserting control cells to the outgoing data stream.

US006151301A

United Stat s Patent [19]

Holden

[11] Patent Number: 6,151,301

[45] Date of Patent: *Nov. 21, 2000

[54] **ATM ARCHITECTURE AND SWITCHING ELEMENT**

[75] Inventor: **Brian D. Holden**, Sunnyvale, Calif.

[73] Assignee: **PMC-Sierra, Inc.**, Burnaby, Canada

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/680,869**

[22] Filed: **Jul. 16, 1996**

Related U.S. Application Data

[63] Continuation of application No. 08/439,078, May 11, 1995, Pat. No. 5,570,348.

[51] Int. Cl.[7] **G06F 11/00; H04L 12/28**

[52] U.S. Cl. **370/232; 370/395; 370/414**

[58] Field of Search 370/229, 230, 370/232, 235, 236, 412, 413–418, 395

[56] **References Cited**

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Badran et al., Head of Line Arbitration in ATM Switches with Input–Output Buffering and Backpressure control Globecom '91, 347–351, Jan. 1991.

Ahmadi, et al., "A Survey of Modern High–Performance Switching Techniques," *IEEE J. of Selected Areas Commun.*, pp. 1091–1103, Sep. 1989, reprinted in *Performance Evaluation*, pp. 4–16.

Alles, "Tutorial: ATM in Private Networking," *Hughes LAN Systems*, 1993.

Chen, et al., "Performance Study of an Input Queuing Packet Switch with Two Priority cases," *IEEE Trans. Commun.*, pp. 117–126, Jan. 1991, reprinted in *Performance Evaluation*, pp. 99–107.

Fujitsu (pub.), *Asynchronous Transfer Mode: IC's for ATM*, 1993.

IEEE Press (pub.), *Performance Evaluation of High Speed Switching Fabrics and Networks*, Roberiazzi (ed.), pp. 1–3, 251–252, 1993.

Karol, et al., "Input Versus Output Queuing on a Space Division Packet Switch," *IEEE Trans. Commun.*, pp.1347–1356, Dec. 1987, reprinted in *Performance Evaluation*, pp. 59–68.

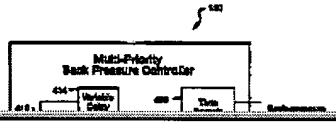
Kim, et al., "Call Scheduling Algorithms in a Multicast Switch," *IEEE Trans. Commun.*, pp. 625–635, Mar. 1992, reprinted in *Performance Evaluation*, pp. 290–299.

Primary Examiner—Chau Nguyen
Assistant Examiner—Phuongchau Ba Nguyen
Attorney, Agent, or Firm—Townsend & Townsend and Crew LLP; Kenneth R. Allen

[57] **ABSTRACT**

An ATM switching system architecture of a switch fabric-type is built of, a plurality of ATM switch element circuits and routing table circuits for each physical connection to/from the switch fabric. A shared pool of memory is employed to eliminate the need to provide memory at every crosspoint. Each routing table maintains a marked interrupt linked list for storing information about which ones of its virtual channels are experiencing congestion. This linked list is available to a processor in the external workstation to alert the processor when a congestion condition exists in one of the virtual channels. The switch element circuit typically has up to eight 4-bit-wide nibble inputs and eight 4-bit-wide nibble outputs and is capable of connecting cells received at any of its inputs to any of its outputs, based on the information in a routing tag uniquely associated with each cell.

4 Claims, 13 Drawing Sheets



US-PAT-NO: 5673255

DOCUMENT-IDENTIFIER: US 5673255 A

TITLE: Apparatus for providing service to telephone subscribers connected to a remote terminal from multiple telephone service providers

---------- KWIC ---------

Brief Summary Text - BSTX (14):

This problem is solved and a technical advance is achieved in the art by a system and method that permits competitive access providers the ability to provide service to subscriber lines connected to a remote terminal, and the ability to control and test such lines. According to this invention, a new unbundling apparatus is inserted between a host switch and a remote terminal in order to provide access to voice channels, maintenance channels, and the control channel for competitive access providers. This remote terminal unbundling apparatus includes a switch fabric, a command module, and a testing module. In configurations where the remote terminal is connected directly to the switch, (i.e., FIG. 1) the unbundling apparatus is merely inserted somewhere in the channel path. Thus, all voice and control channels which were formerly attached between the remote terminal and the host switch are connected through the switch fabric, and the testing line from the remote terminal to the switch is connected through the testing module. Competitive access providers can then connect voice and control channels to the switch fabric which may then be connected to the remote terminal, and a testing line from each of the competitive access providers is connected to the remote terminal via the testing module.

Brief Summary Text - BSTX (15):

The switch fabric of the unbundling apparatus connects all voice channels between the remote terminal and all service providers. It also switches the control channels between the LEC switch and the competitive access providers on the one hand and the remote terminal on the other to the command module. The command module performs any protocol translations necessary (such as TR08 to TR303). All control messages from switches are then multiplexed and sent back to the switch fabric, which routes them to the original command channel to the

US005673255A

United States Patent [19]

Dunn et al.

[11] Patent Number: 5,673,255

[45] Date of Patent: Sep. 30, 1997

[54] **APPARATUS FOR PROVIDING SERVICE TO TELEPHONE SUBSCRIBERS CONNECTED TO A REMOTE TERMINAL FROM MULTIPLE TELEPHONE SERVICE PROVIDERS**

[75] Inventors: James Patrick Dunn, Sandwich; William Brohmer Penison, Naperville; Carl Robert Posthuma, Wheaton; Dorothy Voytko Stanley, Warrenville, all of Ill.

[73] Assignee: Lucent Technologies Inc., Murray Hill, N.J.

[21] Appl. No.: 580,240

[22] Filed: Dec. 28, 1995

[51] Int. Cl.[6] H04Q 1/20; H04Q 3/58

[52] U.S. Cl. 370/244; 370/360; 370/467; 379/14

[58] Field of Search 370/241, 242, 370/244, 247, 357, 360, 373, 377, 384, 378, 466, 467, 522, 525; 379/27.9, 12, 14, 29, 15, 207, 219, 229, 230, 231, 232

[56] References Cited

U.S. PATENT DOCUMENTS

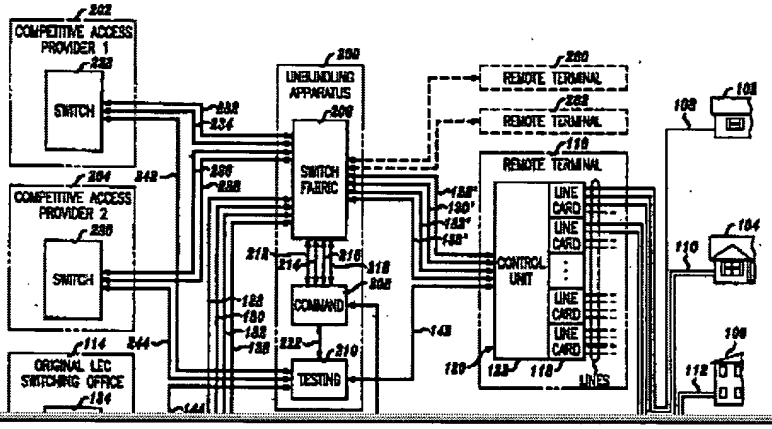
5,119,366 6/1992 Aston et al. 370/378
5,574,783 11/1996 Dunn 379/230

Primary Examiner—Douglas W. Olms
Assistant Examiner—Chau T. Nguyen
Attorney, Agent, or Firm—Michael B. Johannesen

[57] ABSTRACT

An unbundling apparatus to permit competitive access providers access to telephone lines connected to a remote terminal, and the ability to control and test such lines. Such unbundling apparatus includes a switch fabric, a command module, and a testing module. The switch fabric provides all voice channel connections between all switches and the remote terminal and grooms the control channels. Control messages are switched into the command module, which performs any protocol translations necessary. All commands from switches are then multiplexed and sent back to the switch fabric, which routes them to the original command channel to the remote terminal. Control messages from the remote terminal are demultiplexed, translated (if necessary) and sent to the switch fabric for delivery to the appropriate switch. Testing of lines is also provided to all competitive service providers.

12 Claims, 14 Drawing Sheets



US-PAT-NO: 5583861

DOCUMENT-IDENTIFIER: US 5583861 A

TITLE: ATM switching element and method having independently accessible cell memories

---------- KWIC ---------

Detailed Description Text - DETX (8):

FIG. 4 is a block diagram of a routing table circuit 42 according to the present invention. The routing table circuit 42 is a combination storage and control device that is used with external memory, e.g., SRAM 90, and includes a receive queue controller 80 which sends data to the switch fabric and receives a back-pressure signal from the switch fabric, and a transmission buffer controller 82 which receives data from the switch fabric after that data has been processed by the multicast header translation circuit 84 and asserts back pressure to the switch fabric. The transmission buffer controller 82 also includes a small buffer memory 86 for storing cells received from the switch fabric. A further controller, called a connection table controller 88, is for reading header information from the workstation interface and is operative to use that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Controller 88 stores information about switch tags and buffers data in external SRAM 90. Further included are an interrupt processor 92 and processor interface 94, which are for sending control signals to the workstation. Optionally included is an OAM.backslash.BECN cell transmit circuit 96 for inserting control cells to the outgoing data stream.

US005583861A

United States Patent [19]

Holden

[11] Patent Number: 5,583,861

[45] Date of Patent: Dec. 10, 1996

[54] **ATM SWITCHING ELEMENT AND METHOD HAVING INDEPENDENTLY ACCESSIBLE CELL MEMORIES**

[75] Inventor: Brian D. Holden, Sunnyvale, Calif.

[73] Assignee: Integrated Telecom Technology, Santa Clara, Calif.

[21] Appl. No.: 235,006

[22] Filed: Apr. 28, 1994

[51] Int. Cl.[6] H04L 12/54

[52] U.S. Cl. 370/398; 370/352; 370/412; 370/419

[58] Field of Search 370/60, 60.1, 61, 370/85.6, 94.1

[56] References Cited

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Karol et al., "Input Versus Output Queuing on a Space Division Packet Switch", *IEEE Trans. Commun.*, Dec. 1987, pp. 1347–1356, reprinted in *Performance Evaluation*, pp. 59–68.

Chen et al., "Performance Study of an Input Queuing Packet Switch with Two Priority Cases", *IEEE Trans. Commun.*, Jan. 1991, pp. 117–126, reprinted in *Performance Evaluation*, pp. 99–107.

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Yeh et al., "The Knockout Switch: A Simple, Modular Architecture for High Performance Packet Switching", *IEEE J. Selected Areas Commun.*, Oct. 1987, pp. 1274–1283, reprinted in *Performance Evaluation*, pp. 223–234.

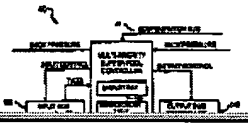
(List continued on next page.)

Primary Examiner—Douglas W. Olms
Assistant Examiner—Russell W. Blum
Attorney, Agent, or Firm—Townsend and Townsend and Crew, LLP

[57] **ABSTRACT**

An ATM switching system architecture of a switch fabric-type is built of, a plurality of ATM switch element circuits and routing table circuits for each physical connection to/from the switch fabric. A shared pool of memory is employed to eliminate the need to provide memory at every crosspoint. Each routing table maintains a marked interrupt linked list for storing information about which ones of its virtual channels are experiencing congestion. This linked list is available to a processor in the external workstation to alert the processor when a congestion condition exists in one of the virtual channels. The switch element circuit typically has up to eight 4-bit-wide nibble inputs and eight 4-bit-wide nibble outputs and is capable of connecting cells received at any of its inputs to any of its outputs, based on the information in a routing tag uniquely associated with each cell.

15 Claims, 13 Drawing Sheets



US-PAT-NO: 5557607

DOCUMENT-IDENTIFIER: US 5557607 A

TITLE: Methods and apparatus for enqueueing and dequeueing data cells in an ATM switch fabric architecture

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Detailed Description Text - DETX (8):

FIG. 4 is a block diagram of a routing table circuit 42 according to the present invention. The routing table circuit 42 is a combination storage and control device that is used with external memory, e.g., SRAM 90, and includes a receive queue controller 80 which sends data to the switch fabric and receives a back-pressure signal from the switch fabric, and a transmission buffer controller 82 which receives data from the switch fabric after that data has been processed by the multicast header translation circuit 84 and asserts back pressure to the switch fabric. The transmission buffer controller 82 also includes a small buffer memory 86 for storing cells received from the switch fabric. A further controller, called a connection table controller 88, is for reading header information from the workstation interface and is operative to use that header information to add an appropriate switch tag to the cells before they are transmitted to the switch fabric. Controller 88 stores information about switch tags and buffers data in external SRAM 90. Further included are an interrupt processor 92 and processor interface 94, which are for sending control signals to the workstation. Optionally included is an OAM/BECN cell transmit circuit 96 for inserting control cells to the outgoing data stream.

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L5: Entry 17 of 17 File: USPT Sep 17, 1996

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TITLE: Methods and apparatus for enqueueing and dequeueing data cells in an ATM switch fabric architecture

DATE-ISSUED: September 17, 1996

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APPL-NO: 08/ 439147 [PALM]
DATE FILED: May 11, 1995

PARENT-CASE:
This a Division of application Ser. No. 08/235,006 filed Apr. 28, 1994

INT-CL: [06] H04 L 12/64

US-CL-ISSUED: 370/58.2; 370/60.1, 370/61, 370/85.6, 370/94.2, 340/825.5
US-CL-CURRENT: 370/413; 340/825.5, 370/395.31, 370/395.4, 370/395.7

FIELD-OF-SEARCH: 370/58.2, 370/60, 370/60.1, 370/61, 370/85.2, 370/85.6, 370/94.1, 370/94.2, 340/825.5, 340/825.51

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

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☐	5126999	June 1992	Munter et al.	370/60
☐	5241536	August 1993	Grimble et al.	370/60.1
☐	5278828	January 1994	Chao	370/85.6

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☐	5299190	March 1994	LaMaire et al.	370/58.2
☐	5303078	April 1994	Bracket et al.	370/60.1 X

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ART-UNIT: 263

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ABSTRACT:

An ATM switching system architecture of a switch fabric-type is built of, a plurality of ATM switch element circuits and routing table circuits for each physical connection to/from the switch fabric. A shared pool of memory is employed to eliminate the need to provide memory at every crosspoint. Each routing table maintains a marked interrupt linked list for storing information about which ones of its virtual channels are experiencing congestion. This linked list is available to a processor in the external workstation to alert the processor when a congestion condition exists in one of the virtual channels. The switch element circuit typically has up to eight 4-bit-wide nibble inputs and eight 4-bit-wide nibble outputs and is capable of connecting cells received at any of its inputs to any of its outputs, based on the information in a routing tag uniquely associated with each cell.

11 Claims, 18 Drawing figures